WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first impurity doped region of a second conductivity type formed in a semiconductor substrate of a first conductivity type;

a second impurity doped region of the first conductivity type formed in the semiconductor substrate of the first conductivity type;

a first gate insulation film formed on the first impurity doped region;

a first gate electrode formed on the first gate insulation film;

a second gate insulation film formed on the second impurity doped region;

a second gate electrode formed on the second gate insulation film;

a first sidewall insulation film formed on either side of the first gate electrode;

a second sidewall insulation film whose thickness differs from that of the first sidewall insulation film, the second sidewall insulation film being formed on either side of the second gate electrode;

a third sidewall insulation film formed on the first sidewall insulation film on the side of the first gate electrode; and

a fourth sidewall insulation film whose thickness differs from that of the third sidewall insulation

film, the fourth sidewall insulation film being formed on the second sidewall insulation film on the side of the second gate electrode.

2. The semiconductor device according to claim 1, wherein the second sidewall insulation film is thinner than the first sidewall insulation film.

3. The semiconductor device according to claim 2, wherein the fourth sidewall insulation film is thinner than the third sidewall insulation film.

4. The semiconductor device according to claim 1, wherein:

the first sidewall insulation film is an offset spacer used to form a first extension region in the first impurity doped region, a first channel region formed beneath the first gate insulation film being interposed between the first extension region; and

the second sidewall insulation film is an offset spacer used to form a second extension region in the second impurity doped region, a second channel region formed beneath the second gate insulation film being interposed between the second extension regions.

5. The semiconductor device according to claim 4, wherein:

the third sidewall insulation film is a gate sidewall film used to form a first source/drain region in the first impurity doped region and outer side of each of the first extension regions between which the

first channel region is interposed; and

the fourth sidewall insulation film is a gate sidewall film used to form a second source/drain region in the second impurity doped region and outer side of each of the second extension regions between which the second channel region is interposed.

6. The semiconductor device according to claim 5, wherein:

the first gate electrode, the first gate insulation film, the first extension regions, and the first source/drain region make up a p-channel MOS field effect transistor in the first impurity doped region of the second conductivity type; and

the second gate electrode, the second gate insulation film, the second extension regions, and the second source/drain region make up an n-channel MOS field effect transistor in the second impurity doped region of the first conductivity type.

7. The semiconductor device according to claim 1, further comprising an isolation region which isolates the first impurity doped region and the second impurity doped region from each other.

8. The semiconductor device according to claim 1, wherein the second sidewall insulation film contains an element which enhances an etching rate over that of the first sidewall insulation film.

9. The semiconductor device according to claim 8,

wherein the fourth sidewall insulation film contains an element which enhances an etching rate over that of the third sidewall insulation film.

10. The semiconductor device according to claim 1, wherein the second gate electrode contains an element which is not contained in the first gate electrode.

11. The semiconductor device according to claim 9, wherein the element is at least one of arsenic, phosphorus, boron, indium, carbon and germanium.

12. The semiconductor device according to claim 10, wherein the element is at least one of arsenic, phosphorus, boron, indium, carbon and germanium.

13. The semiconductor device according to claim 1, wherein the first sidewall insulation film and the second sidewall insulation film each include one of a TEOS film and a silicon nitride film.

14. The semiconductor device according to claim 13, wherein the third sidewall insulation film and the fourth sidewall insulation film each include a multilayer film which is made up of a TEOS film, a silicon nitride film and a BSG film.

15. A method of manufacturing a semiconductor device, comprising:

forming a first gate electrode on a first impurity doped region of a second conductivity type in a semiconductor substrate of a first conductivity type;

forming a second gate electrode on a second impurity doped region of the first conductivity type in the semiconductor substrate;

forming a first insulation film on the first and second gate electrodes and the first and second impurity doped regions;

introducing an element, which varies an etching rate of the first insulation film, only into the first insulation film formed on the second impurity doped region and the second gate electrode;

processing the first insulation film by anisotropic etching to form a first sidewall insulation film on either side of the first gate electrode and a second sidewall insulation film on either side of the second gate electrode, the second sidewall insulation film having a thickness different from that of the first sidewall insulation film;

forming a third impurity doped region of the first conductivity type in the first impurity doped region by ion implantation using the first gate electrode and the first sidewall insulation films as a mask; and

forming a fourth impurity doped region of the second conductivity type in the second impurity doped region by ion implantation using the second gate electrode and the second sidewall insulation films as a mask.

16. The method according to claim 15, further

comprising:

forming a second insulation film on the semiconductor substrate after the third and fourth impurity doped regions are formed;

introducing an element, which varies an etching rate of the second insulation film, only into the second insulation film formed on the second and fourth impurity doped regions and the second gate electrode;

processing the second insulation film by anisotropic etching to form a third sidewall insulation film on the first sidewall insulation film on the side of the first gate electrode and a fourth sidewall insulation film on the second sidewall insulation film on the side of the second gate electrode, the fourth sidewall insulation film having a thickness different from that of the third sidewall insulation film;

forming a fifth impurity doped region of the first conductivity type in the first impurity doped region by ion implantation using the first gate electrode, the first sidewall insulation film and the third sidewall insulation film as a mask; and

forming a sixth impurity doped region of the second conductivity type in the second impurity doped region by ion implantation using the second gate electrode, the second sidewall insulation film and the fourth sidewall insulation film as a mask.

17. The method according to claim 15, wherein

the second sidewall insulation film is thinner than the first sidewall insulation film.

18. The method according to claim 16, wherein the fourth sidewall insulation film is thinner than the third sidewall insulation film.

19. The method according to claim 15, wherein the element which varies the etching rate is an element which enhances the etching rate.

20. The method according to claim 19, wherein the element which enhances the etching rate is at least one of arsenic, phosphorus, boron, indium, carbon and germanium.

21. A method of manufacturing a semiconductor device, comprising:

forming first and second element forming regions in a semiconductor substrate of a first conductivity type, the first and second element forming regions being isolated from each other by an isolation region;

forming a first impurity doped region of a second conductivity type in the first element forming region;

forming a second impurity doped region of the first conductivity type in the second element forming region;

forming first and second gate insulation films on the first and second impurity doped regions, respectively;

forming first and second gate electrodes on

the first and second gate insulation films, respectively;

forming a first insulation film on the first and second gate electrodes and the first and second impurity doped regions;

introducing an element, which varies an etching rate of the first insulation film, only into the first insulation film formed on the second impurity doped region; and the second gate electrode;

processing the first insulation film by anisotropic etching to form a first offset spacer on either side of the first gate electrode and a second offset spacer on either side of the second gate electrode, the second offset spacer having a thickness different from that of the first offset spacer;

forming a first extension region of the first conductivity type in the first impurity doped region by ion implantation using the first gate electrode and the first offset spacer as a mask; and

forming a second extension region of the second conductivity type in the second impurity doped region by ion implantation using the second gate electrode and the second offset spacer as a mask.

22. The method according to claim 21, further comprising:

forming a second insulation film on the first and second impurity doped regions and the first and second

gate electrodes after the first extension region and the second extension region are formed;

introducing an element, which varies an etching rate of the second insulation film, only into the second insulation film formed on the second impurity doped region and the second gate electrode;

processing the second insulation film by anisotropic etching to form a first gate sidewall film on the first offset spacer on the side of the first gate electrode and a second gate sidewall film on the second offset spacer on the side of the second gate electrode, the second gate sidewall film having a thickness different from that of the first gate sidewall film;

forming a first source/drain region of the first conductivity type in the first impurity doped region by ion implantation using the first gate electrode, the first offset spacer, and the first gate sidewall film as a mask; and

forming a second source/drain region of the second conductivity type in the second impurity doped region by ion implantation using the second gate electrode, the second offset spacer, and the second gate sidewall film as a mask.